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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/551,324	10/18/2005	Radjindrepersad Gajadharsing	SOROK16.001APC	7460
20995	7590	01/15/2009	EXAMINER	
KNOBBE MARTENS OLSON & BEAR LLP			SALERNO, SARAH KATE	
2040 MAIN STREET				
FOURTEENTH FLOOR			ART UNIT	PAPER NUMBER
IRVINE, CA 92614			2814	
			NOTIFICATION DATE	DELIVERY MODE
			01/15/2009	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jcartee@kmob.com  
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<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/551,324	GAJADHARSING ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	SARAH K. SALERNO	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 15 December 2008.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-11 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ .  | 6) <input type="checkbox"/> Other: _____ .                        |

## DETAILED ACTION

1. Applicant's amendment/arguments filed on 05/15/08 and 12/15/08 as being acknowledged and entered. By this amendment no claims are canceled, no new claims have been added, claims 1-11 are pending and no claims are withdrawn.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-11 rejected under 35 U.S.C. 103(a) as being unpatentable over Jos (US Patent 6,069,386) in view of Yokayama et al. (US PGPub 2002/0003247).

Claim 1: Jos teaches a semiconductor device comprising a semiconductor body (1) which is provided with a field effect transistor at a surface and which comprises strongly doped source (4) and drain zones (5) and a channel region extending between the source zone and the drain zone (Col. 2 lines 50-67), with a gate electrode (9) being present which overlaps the channel region upon perpendicular projection thereon, wherein the source zone (4), the drain zone (5) and the gate electrode (9) are connected at the surface to a metal source contact (15), a drain contact (16) and a gate electrode contact (18), respectively via metal strips, and wherein a further metal strip (20) is positioned between the gate electrode contact (18) and the drain contact (16), which further metal strip is insulated from the semiconductor body (14), is locally

electrically connected to the metal source contact (15), and forms a shield between the gate electrode (18) and the drain contact (16) (Col. 3 lines 45-50), and in that the further metal strip is provided with a connecting contact (12) for applying an external voltage to the further metal strip (20) (Col. 3 lines 9-12, 25-27 & 51-53) (FIG. 1-3).

Jos does not teach the electrical connection between the further metal strip (524) and the metal source contact (515) comprises a capacitor. Yokayama teaches an electrical connection between a metal source contact and further metal strip comprises a capacitor to improve device performance (FIG. 22C; [0004, 0192-0200]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the electrical connection taught by Jo to be a capacitor to improve device performance as taught by Yokayama (FIG. 22C; [0004, 0192-0200]).

Claim 2: Jos teaches the capacitor is integrated in the semiconductor body (1) and is positioned within the active region beside the transistor (FIG. 2).

Claim 3: Jos teaches the source contact (15), the drain contact (16), the gate electrode contact (18), the further metal strip (20) and the connecting contact thereof (12), are formed in a first metal layer. Zambrano teaches an electrode of the capacitor (20) is formed in a second metal layer arranged above the first metal layer, and wherein the first and second metal layers are separated from one another by a further insulating layer (7) (FIG. 2-3).

Claim 4: Jos teaches the other electrode of the capacitor (15) is formed by the semiconductor body (1), which comprises a strongly doped substrate (2) on which a more weakly doped epitaxial layer is present (3) (FIG. 2-3).

Claim 5: Jos teaches the two electrodes of the capacitor form part of the metal layers, and the lower electrode (15) of said two electrodes is electrically connected to the semiconductor body (1), which comprises a strongly doped region (11) at that location (FIG. 2).

Claim 6: Jos teaches a semiconductor device operating the device at 2Ghz, which falls within the claimed frequency of 100 MHz and 3 GHz. Applicant states in the disclosure that capacitance of the capacitor partially depends on the desired operating frequency (page 4 lines 13-15). Since it has been held when the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 223, 235 (CCPA 1955). Applicant can rebut a prima facie case of obviousness based on ranges by showing unexpected results or the criticality of the claimed range. “The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claim. In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.” In re Woodruff, 919 F. 2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP 716.02-716.02(g) for a discussion of criticality and unexpected results. There is nothing in the present application to indicate that the claimed frequency or capacitance is critical and someone of ordinary skill in the art would have been able to determine, through routine experimentation, the proper capacitance to operate the device successfully based on the operating frequency.

Claim 7: Jos teaches the field effect transistor is a MOS transistor, in which the semiconductor body (1) comprises a comparatively weakly doped region (3) of a first conductivity type (p) adjoining the surface, which region is provided with the strongly doped source (4) and drain zone (5) of the opposed, second conductivity type (n) and a weakly doped drain extension (8) between the drain zone (5) and the channel region, wherein the gate electrode (9) is electrically insulated from the channel region and an electrically insulating layer (14) is laid over the surface, which layer is provided with contact windows above the source zone (4), the drain zone (5) and the gate electrode (9), through which contact windows the source zone (4), the drain zone (5) and the gate electrode (9), respectively, are connected to the contacts (15, 16, 18) (FIG. 2).

Claim 8: Jos teaches the metal strips connecting the source zone, the drain zone and the gate electrode to their respective contacts (16, 18, and 15) are embodied as parallel metal strips positioned beside each other (FIG. 1).

Claim 9: Jos teaches another metal strip (21) is present between the further metal strip (20) and the gate electrode (18), which other strip (21) is separated from the semiconductor body (1) by an electrically insulating layer (14,7) and may or may not be provided with another connecting contact for applying another external voltage (FIG. 1-3).

Claim 10: Jos teaches a voltage is applied to the contact region of the further metal strip during operation of the device (Col. 3 lines 9-12, 25-27 & 51-53).

Claim 11: Jos teaches the applied voltage is selected independence on the power range within which the device operates (Col. 3 lines 9-12, 25-27 & 51-53).

### ***Response to Arguments***

4. Applicant's arguments, filed 12/15/08 have been fully considered and are persuasive. The final action of 8/21/08 has been withdrawn.

***Conclusion***

5. Applicant's amendments on 5/15/08 necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH K. SALERNO whose telephone number is (571)270-1266. The examiner can normally be reached on M-F 8:00-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. K. S./  
Examiner, Art Unit 2814

/Theresa T. Doan/  
Primary Examiner, Art Unit 2814